

# NP75N04VUK

40 V - 75 A - N-channel Power MOS FET Application: Automotive

R07DS0954EJ0100 Rev.1.00 Nov 20, 2012

# **Description**

The NP75N04VUK is N-channel MOS Field Effect Transistor designed for high current switching applications.

### **Features**

• Super low on-state resistance

 $R_{DS(on)}$  = 5.7 mW MAX. (V  $_{GS}$  = 10 V,  $I_{D}$  = 38 A)

- Low  $C_{iss}$ :  $C_{iss} = 1630 \text{ pF TYP.} (V_{DS} = 25 \text{ V})$
- Designed for automotive application and AEC-Q101 qualified

# **Ordering Information**

Part No.	Lead Plating	Pac	Package	
NP75N04VUK-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	TO-252 (MP-3ZP)
NP75N04VUK-E2-AY *1			Taping (E2 type)	

Note: \*1 Pb-free (This product does not contain Pb in the external electrode)

# **Absolute Maximum Ratings** $(T_A = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	40	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC) (T <sub>C</sub> = 25°C)	I <sub>D(DC)</sub>	±75	А
Drain Current (pulse) *1	I <sub>D(pulse)</sub>	±225	А
Total Power Dissipation (T <sub>C</sub> = 25°C)	P <sub>T1</sub>	75	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T2</sub>	1.2	W
Channel Temperature	T <sub>ch</sub>	175	°C
Storage Temperature	T <sub>stg</sub>	-55 to +175	°C
Repetitive Avalanche Current *2	I <sub>AR</sub>	22	Α
Repetitive Avalanche Energy *2	E <sub>AR</sub>	48	mJ

Notes: \*1  $\,T_{C}$  = 25°C,  $P_{W} \leq$  10  $\mu s,\, Duty\,\, Cycle \leq$  1%

# **Thermal Resistance**

<sup>\*2</sup>  $R_G = 25 \Omega$ ,  $V_{GS} = 20 V \rightarrow 0 V$ 

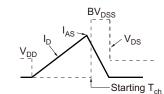
# **Electrical Characteristics** (T<sub>A</sub> = 25°C)

Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	_	_	1	μΑ	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$	
Gate Leakage Current	I <sub>GSS</sub>	_	_	±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	
Forward Transfer Admittance *1	y <sub>fs</sub>	20	40	_	S	$V_{DS} = 5 \text{ V}, I_{D} = 38 \text{ A}$	
Drain to Source On-state Resistance *1	R <sub>DS(on)</sub>	_	4.7	5.7	mΩ	$V_{GS} = 10 \text{ V}, I_D = 38 \text{ A}$	
Input Capacitance	C <sub>iss</sub>	_	1630	2450	pF	V <sub>DS</sub> = 25 V	
Output Capacitance	Coss	_	220	330	pF	$V_{GS} = 0 V$	
Reverse Transfer Capacitance	C <sub>rss</sub>	_	100	180	pF	f = 1 MHz	
Turn-on Delay Time	t <sub>d(on)</sub>	_	15	40	ns	$V_{DD} = 20 \text{ V}, I_D = 38 \text{ A}$	
Rise Time	t <sub>r</sub>	_	5	20	ns	V <sub>GS</sub> = 10 V	
Turn-off Delay Time	t <sub>d(off)</sub>	_	37	80	ns	$R_G = 0 \Omega$	
Fall Time	t <sub>f</sub>	_	5	20	ns		
Total Gate Charge	$Q_G$	_	30	45	nC	V <sub>DD</sub> = 32 V	
Gate to Source Charge	$Q_{GS}$	_	8	_	nC	V <sub>GS</sub> = 10 V	
Gate to Drain Charge	$Q_{GD}$	_	8	_	nC	$I_D = 75 \text{ A}$	
Body Diode Forward Voltage *1	$V_{F(S-D)}$	_	1.0	1.5	V	I <sub>F</sub> = 75 A, V <sub>GS</sub> = 0 V	
Reverse Recovery Time	t <sub>rr</sub>	_	32	_	ns	I <sub>F</sub> = 75 A, V <sub>GS</sub> = 0 V	
Reverse Recovery Charge	Q <sub>rr</sub>	_	32	_	nC	di/dt = 100 A/μs	

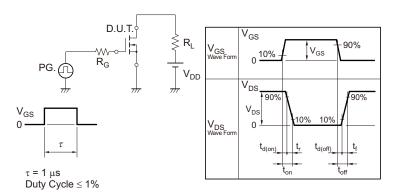
Note: \*1 Pulsed test

# **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

# $V_{GS} = 20 \rightarrow 0 \text{ V}$ $V_{GS} = 20 \rightarrow 0 \text{ V}$



# **TEST CIRCUIT 2 SWITCHING TIME**

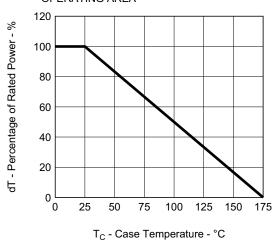


# **TEST CIRCUIT 3 GATE CHARGE**

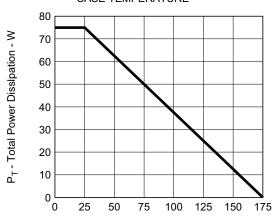
$$\begin{array}{c|c} D.U.T. \\ \hline I_G = 2 \text{ mA} \\ \hline \end{array} \\ \begin{array}{c} PG. \\ \hline \end{array} \\ \begin{array}{c} > 50 \Omega \\ \hline \end{array} \\ \end{array} \\ \begin{array}{c} V_{DD} \\ \hline \end{array}$$

# **Typical Characteristics** $(T_A = 25^{\circ}C)$

# DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

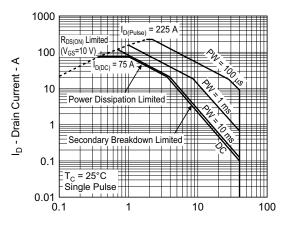


# TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



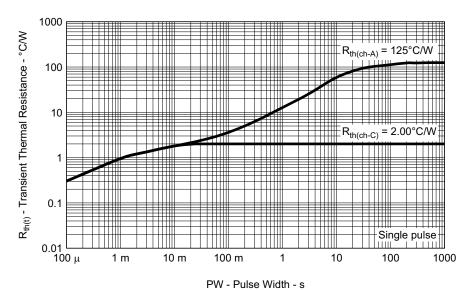
T<sub>C</sub> - Case Temperature - °C

### FORWARD BIAS SAFE OPERATING AREA



V<sub>DS</sub> - Drain to Source Voltage - V

# TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



0

V<sub>GS(th)</sub> - Gate to Source Threshold Voltage - V

 $R_{DS(on)}$  - Drain to Source On-State Resistance -  $m\Omega$ 

0 0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6

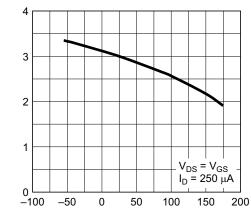
# DRAIN TO SOURCE VOLTAGE 250 200 150 150 V<sub>GS</sub> = 10 V

DRAIN CURRENT vs.

V<sub>DS</sub> - Drain to Source Voltage - V

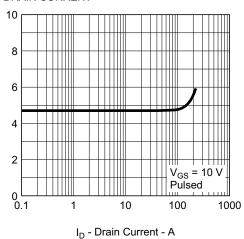
Pulsed

# GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

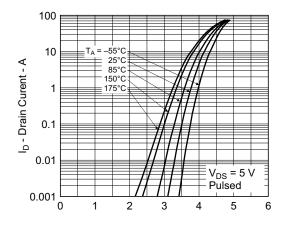


T<sub>ch</sub> - Channel Temperature - °C

# DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

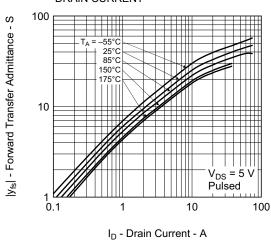


### FORWARD TRANSFER CHARACTERISTICS

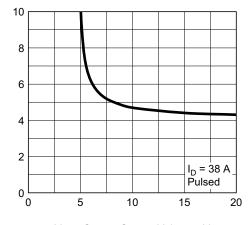


V<sub>GS</sub> - Gate to Source Voltage - V

# FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

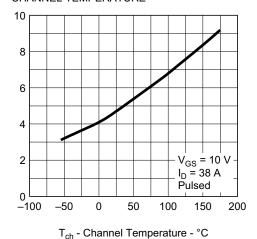


V<sub>GS</sub> - Gate to Source Voltage - V

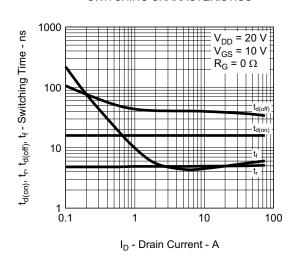
 $R_{\text{DS(on)}}$  - Drain to Source On-State Resistance -  $m\Omega$ 

 $R_{DS(on)}$  - Drain to Source On-State Resistance -  $m\Omega$ 

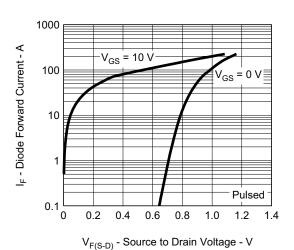
# DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



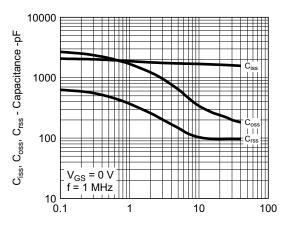
# SWITCHING CHARACTERISTICS



### SOURCE TO DRAIN DIODE FORWARD VOLTAGE

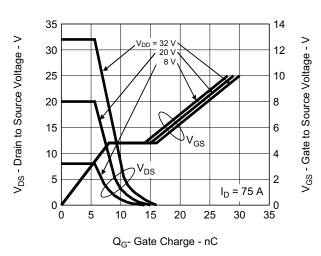


### CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

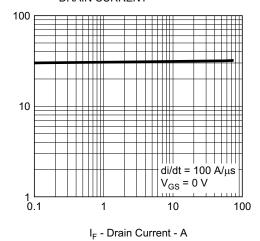


 $V_{DS}$  - Drain to Source Voltage - V

### DYNAMIC INPUT/OUTPUT CHARACTERISTICS



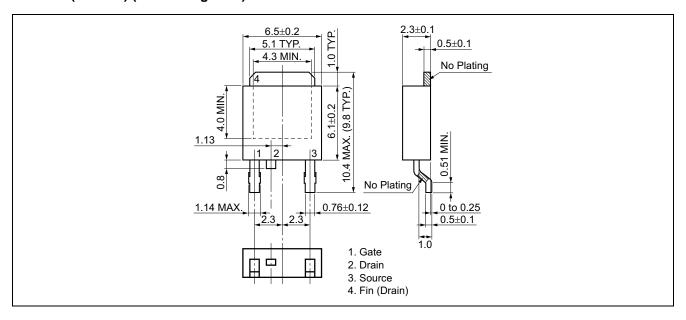
REVERSE RECOVERY TIME vs. DRAIN CURRENT



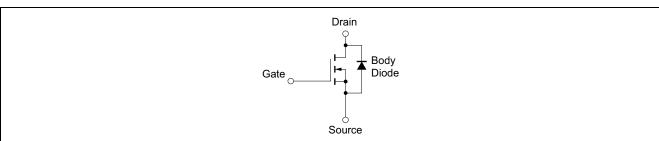
t<sub>rr</sub> - Reverse Recovery Time - ns

# Package Drawing (Unit: mm)

# TO-252 (MP-3ZP) (Mass: 0.3 g TYP.)



# **Equivalent Circuit**



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

**Revision History** 

# NP75N04VUK Data Sheet

		Description		
Rev.	Date	Page	Summary	
1.00	Nov 20, 2012	_	First Edition Issued	

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